REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 10-15 and 17-22 are in this case. Claims 10-15, 17 and 20-22 have been rejected under § 102(b). Claims 10-12, 14, 15 and 17 have been rejected under § 102(e). Claims 13, 18 and 19 have been rejected under § 103(a). Claims 20-22 have been objected to. Claims 12, 17 and 18 have been canceled. Independent claims 10 and 15 and dependent claims 19, 20 and 22 have been amended.

The claims before the Examiner are directed toward a system and method for enabling an executing entity of a host system to directly execute code stored in a non-executable memory component. One or more executable memory components are provided to buffer a portion of the code to an executing entity for direct execution. The executable memory component(s) receive the code directly from the non-executable memory component. When more than one executable memory component is used, then while one executable memory component functions as a buffer of one portion of the code, another portion of the code is downloaded from the non-executable memory component to another executable memory component in order to guarantee continuous access to the code by the executing entity.

§ 102(b) Rejections - Bott

The Examiner has rejected claims 10-15, 17 and 20-22 under § 102(b) as being anticipated by Ed Bott, *Using Windows 95* (Que, 1995) (henceforth, "Bott"). The Examiner's rejection is respectfully traversed.

Claims 12 and 17 have been canceled, thereby rendering moot the Examiner's rejection of these claims.

Bott teaches the basic hardware of a personal computer, including a hard disk that serves as a non-executable memory component for storing code, a CPU that is an executing entity that executes the code and a RAM that serves as an executable memory component for presenting the code to the CPU for execution.

One crucial difference between the present invention and the prior art of Bott is that the executable memory component(s) of the present invention receive(s) the stored code directly from the non-executable memory component. This is in contrast to the situation in a personal computer, in which the RAM receives executable code from the hard disk via a bus that is shared with the CPU, and not directly from the hard disk. See, for example, US 6,434,695, a copy of which is attached. Figure 1 of US 6,434,695 is a high-level block diagram of a typical personal computer **1** such as the Apple Macintosh (column 3 line 7). (Note that the invention of US 6,434,695 is an operating system for such a computer. The hardware illustrated in Figure 1 was in common use long before the December 23, 1998 filing date of US 6,434,695, and was familiar to all those skilled in the art. Applicant presumes that a similar Figure appears in Bott.) Personal computer **1** includes a CPU **10**, a RAM **12** and a mass storage device **13** that communicate with each other via a commonly shared bus system **18**.

While continuing to traverse the Examiner's rejections, Applicant has, in order to expedite the prosecution, chosen to amend independent claim 10 in order to clarify and emphasize this crucial distinction between the device of the present invention and the teachings of Bott. Specifically, independent claim 10 has been amended to recite that each executable memory component receives the stored code directly from the non-executable memory component.

Support for this amendment is found in the specification in Figure 2 and on page 10 line 11. Figure 2 has an arrow from NAND array **30** to executable buffer/s **20** indicating data flow directly from NAND array **30** to executable buffer/s **20**, rather than via the address bus and the data bus shown in the lower part of the Figure. That this arrow indicates a feature of the hardware of the present invention, and is not merely a conceptual symbol to indicate data flow, is shown by page 10 line 11, which states that Figure 2 illustrates "architecture".

Amended independent claim 10 now features language which makes it absolutely clear that the executable memory component(s) receive(s) code directly from the non-executable memory component. Applicant believes that the amendment of the claims completely overcomes the Examiner's rejections on § 102(b) grounds.

With independent claim 10 allowable over Bott in its present form, it follows that claims 11, 13 and 14, that depend therefrom, also are allowable over Bott.

As discussed below, independent claim 15 has been placed in condition for allowance by the inclusion therein of the limitations of claim 18. It follows that claims 20-22, that depend therefrom, also are allowable.

§ 102(e) Rejections – Hwang '399

The Examiner has rejected claims 10-12, 14, 15 and 17 under § 102(e) as being anticipated by Hwang, US Patent No. 6,263,399 (henceforth, "Hwang '399"). The Examiner's rejection is respectfully traversed.

Claims 11, 12 and 17 have been canceled, thereby rendering moot the Examiner's rejection of these claims.

Hwang '399 teaches a memory interface 24 that acts as an intermediary between a CPU **10** and a NAND flash memory **26**. As noted in column 6 line 23,

memory interface **24** could include RAM; and this RAM could be used for direct execution of code from NAND flash memory **26** by CPU **10**.

One feature of the present invention that is lacking in the teachings of Hwang '399 is the feature recited in dependent claim 12: a mechanism for guaranteeing availability in an executable memory component of code requested by the executing entity. The Examiner has asserted that the mere presence of RAM in memory interface **24** guarantees the availability of code from NAND flash memory **26** for CPU **10** to execute. This is not the case. It also is necessary, when the code requested by CPU **10** for execution is not yet stored in the RAM, to indicate to CPU **10** that CPU **10** needs to wait for the requested code to be downloaded from NAND flash memory **26**. Hwang '399 is silent on this issue. Thus, the present invention, as recited in dependent claim 12, is not anticipated from Hwang '399. Furthermore, the present invention, as recited in dependent claim 12, is not even obvious from Hwang '399. The general thrust of Hwang '399 is towards the translation of signals from CPU **10** into a form that NAND flash memory **26** understands. This is stated *inter alia* in column 5 lines 20-24:

> The key to the present invention is that memory interface **24** translates the communication protocol used by the CPU into a form usable by NAND flash memory **26** memory interface **24** communicates with both CPU **10** and NAND flash memory **26** in their native form.

There is neither a hint nor a suggestion in Hwang '399 of either the necessity of indicating to CPU **10** to wait for code to be downloaded from NAND flash memory **26** or of how to accomplish this. Therefore, independent claim 10 has been amended to include the limitation of dependent claim 12. Correspondingly, dependent claim 12 has been canceled.

Amended independent claim 10 now features language which makes it absolutely clear that the device of the present invention includes a mechanism for

guaranteeing the availability of requested code in one of the executable memory components. Applicant believes that the amendment of the claims completely overcomes the Examiner's rejections on § 102(e) grounds.

The Examiner has noted, in the context of the § 103(a) rejections, that both Arakawa et al., US Patent No. 5,590,073 (henceforth, "Arakawa et al. '073") and Nojima, US Patent No. 6,246,634 (henceforth, "Nojima '634") teach the use of Busy/Ready control signals. The mechanism, for guaranteeing availability of code in an executable entity, that is described in the specification on page 9 line 17 through page 10 line 2, relies on busy signals. Ostensibly, this mechanism could be construed as an obvious combination of the teachings of Hwang '399 and either Arakawa et al. '073 or Nojima '634. But as noted in MPEP 706.02(j), for two references to be combined to reject a claim as obvious,

> ...there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

In this case, because Hwang '399 is silent on the subject of how to use memory interface **24** to present executable code (as opposed to data generally) from NAND flash memory **26** to CPU **10**, such a suggestion or motivation is lacking. Therefore, a rejection of dependent claim 12 under § 103(a) as unpatentable over Hwang '399 in view of either Arakawa et al. '073 or Nojima '634 would constitute impermissible hindsight on the part of the Examiner.

With independent claim 10 allowable over Hwang '399 in its present form, it follows that claim 14 that depends therefrom also is allowable over Hwang '399.

As discussed below, independent claim 15 has been placed in condition for allowance by the inclusion therein of the limitations of claim 18.